Manufacturing Support Program

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with International SEMATECH to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain."

Factory Time Synchronization Standards Development for e-Manufacturing

Technical Contact:
Y. Li

Goals

The project's objective is to educate the industry about the requirements, related issues , potential solutions, and standards recommendations to achieve reliable clock synchronization and time stamping capabilities for supporting present and future e-Manufacturing needs.

Customer Needs

Increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Manufacturing of 300 mm semiconductors will require data to be collected and analyzed from a rising confluence of data streams, due to additional sources previously thought to have little impact on manufacturing. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

One of the projected near term Factory Integration difficult challenges in the International Technology Roadmap for Semiconductors (ITRS) is the:

"Explosive growth of data collection/analysis requirements driven by process and modeling nee ..." 2004 ITRS Update, Factory Integration, p. 2.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data.

The completion of the suite of Equipment Data Acquisition standards promises to create a data explosion. With data collection rates increasing to 10,000 data points per second, one millisecond time stamp accuracy will be required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require clock synchronization of all the related local clocks in the manufacturing site including the clocks within the process and metrology tools.

Technical Strategy

Through collaborations with International SEMATECH Manufacturing Initiative (ISMI), this project will investigate and document key issues related to clock synchronization and time stamping internal to the equipment, where the greatest need for accurate time stamps are required. Current time stamp accuracy capabilities, issues preventing the dissemination of accurate timestamps and industry requirements are being gauged based on inputs from network engineers and information technology (IT) managers from chip manufacturers. Feedback from equipment suppliers also provides insight into current architectural issues preventing tools from providing accurate clock synchronization and time stamping. Software suppliers for process analysis tools will also be able to provide insight on current limitations due to inaccurate time stamps. A review of how other industries relying on process control data have addressed the clock synchronization and time stamping issue will also provide some guidelines of how the semiconductor industry can evolve to adopt an accurate time stamping mechanism.

DELIVERABLES: Document factory and equipment clock synchronization and time stamping recommendations based on semiconductor industry needs and lessons learned from other manufacturing industries. 3Q 2005

To achieve accurate timestamps, it is imperative to have a reliable and accurate clock synchronization methodology. The industry should understand how to obtain and distribute accurate time

throughout their factory networks. Network Time Protocol (NTP) and IEEE 1588 Precision Time Protocol (PTP) for industrial sensor networks are two of the key protocols for potential use in the semiconductor industry. A small network of NTP servers will be established to estimate its accuracy capabilities under different configurations to determine the effects of network and processor load on synchronization accuracy. Findings from the experiment will reveal some best methods for NTP use. The project will also continue to follow developments in PTP and participate in the IEEE 1588 User Requirements task force.

DELIVERABLES: Document current clock synchronization technologies by including a cookbook and best practices for NTP and a review of latest developments in IEEE 1588. 4Q 2005

Consistent time stamping formats must also be established, and the project will look at some of the widely used formats available such as ISO 8601. Semiconductor Equipment Materials International (SEMI) standards related to clock models and communication of synchronization and time stamping information will be reviewed to identify the standards to be modified or added to promote accurate clock synchronization among equipment subsystems and within the factory.

Accomplishments

- A NIST internal report (NISTIR 7184) on "Semiconductor Factory and equipment Clock Synchronization for e-Manufacturing" was published in December 2004.

- The presentation on "*Running Out of Time:* Improvements Required in Current Semiconductor and Equipment Clock Synchronization for Supporting Future Real-Time Data Collection" was given at AEC/APC Symposium in September 2004.

- An educational presentation was given on time synchronization issues and potential solutions at the SEMI International Equipment Engineering Task Force at SEMICON West in July 2004.

Collaborations

Harvey Wohlwend, Brad Van Eck, Gino Crispieri, International SEMATECH Manufacturing Initiative

Engineering Chain Management in the Semiconductor Industry

Technical Contacts:
J. Messina
K. Brady

Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry's hopes to reduce time, inventory, and therefore costs.

"It is expected that improvements in manufacturing productivity will play an even greater future role in reducing time to money and getting the most out of factory investment." 2004 International Technology Roadmap for Semiconductors Factory Integration (ITRS) Overview Update, p.52.

The transition to 300 mm fabs and single-wafer lots has challenged the semiconductor industry in nearly every aspect of production, such as: facility layout; the mix of R&D within a single fab; data analysis of small lots; tool to tool interconnect; automated material handling and tracking of product, non-product wafers and reticles; the division of the production process across a partnership of foundries, designers, production sites, distributors and equipment manufacturers. Chip manufacturers require greater visibility of end product demand to accurately schedule their factories, and require greater technical collaboration with designers, OEMs, and foundries to ensure the manufacturability of the product being designed today using the generation of equipment that will be installed once production starts.

Cost of design is the greatest threat to continuation of the semiconductor roadmap. 2003 ITRS, p. 1.

According to the 2001 ITRS, design complexity has been growing exponentially due to the increasing density and number of transistors to meet performance goals. Intellectual Property (IP) reuse helps companies get complex systems to market quickly by eliminating redundant design effort. Standard formats for IP specifications and tool interfaces for the design of a System-on-a-Chip (SoC) would reduce time to market by eliminating the need for translations. Security mechanisms must also be incorporated to protect IP during transfers.

Other information-exchange gaps in design houses include standard data formats for timing and power to expedite timing closure, reduce design iterations, and promote interoperability among best-of-breed software tools.

The industry trend towards outsourcing is leading towards silos of expertise, exactly when technology advances require a multi-disciplinary approach to problem solving. The production process is being conducted across fabs – not only at the traditional point of packaging and test, but mid-stream in the IC fabrication process. As the wafers change hands, so must the information about that wafer which accumulated during its production life cycle.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES: Contribute to the update of the Factory Integration component of the ITRS by co-leading the Engineering Chain Management subteam.
4Q 2005

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as Inter-national SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current

areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES: Establish a working agreement with ISMT in order to identify top industry IT-standards related needs and develop potential solutions to the current challenges based on cross-industry solutions facing similar issues. 3Q 2005

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Provide technical assistance to facilitate current IT standards development efforts within the semiconductor industry by participating in ISMT and SEMI standards activities. 4Q 2005

Accomplishments

- Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial has been taught as a class at both NIST and various SEMI standards workshops.

- Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.

- NIST has been co-leading the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Initial efforts are being made to determine the scope and identify the challenges of creating an effective Engineering Chain.

- Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Collaborations

Alan Weber, Alan Weber & Associates

ITRS Factory Integration Technical Working Group

SEMI XML Task Force

International SEMATECH (ISMT)

NIST/SEMATECH e-Handbook of Statistical Methods

Goals

The goal of the *NIST/SEMATECH e-Handbook of Statistical Methods* project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the *e-Handbook* readily accessible to its target audiences in industry, including the semiconductor manufacturing industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

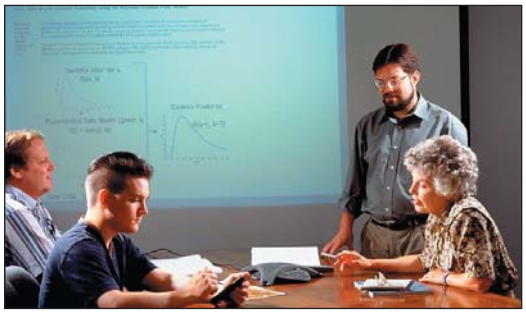
Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

DELIVERABLES: Update and maintain the e-Handbook on-line, and continue to distribute the e-Handbook on CD for off-line use. 4Q 2005

Accomplishments

Since release of the final version, work has focused on publicizing the *e-Handbook*, responding to user feedback, and developing a compact disk version for off-line use. The web version of the e-Handbook averages approximately 1 million hits per month and over 6,000 e-Handbook compact disks have been distributed to industrial, government, and academic users all over the world over the last two years. Publicity on the e-Handbook has appeared in *Science*, *Quality Digest*, *MicroMagazine.com*, *States News Service*, *National Science Digital Library Report for Math, Engineering, and Technology*, and *American Statistician*.



NIST e-Handbook of Statistical Methods team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

Collaborations

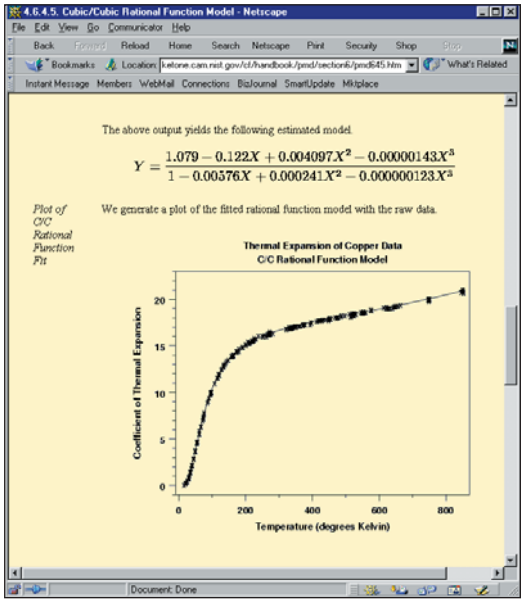
International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

Recent Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.



Page from a case study in the process modeling chapter of the Handbook.

Technical Contacts:
W. F. Guthrie
A. Heckert
J. J. Filliben

"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc.